

Technical Notes on using Analog Devices' DSP components and development tools

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ADSP-21161: Recommended Handling of Unused Pins

Introduction

The ADSP-21161 (SHARC) processors contain 225 pins offered in either a 17 mm x 17 mm PBGA or MBGA package. Many of these pins are only necessary for specific functions, such as the serial ports, link ports or SPI signals. If your application does not make use of a peripheral feature, the associated signals (pins) may still require a connection rather than be left floating (unconnected). This EE-Note suggests recommended methods of handling the pins associated with unused functions. Compared to previous SHARC DSPs, the ADSP-21161 has some modifications in the internal I/O drivers that the DSP hardware designer should be aware of, especially if migrating from a previous SHARC-based design. This information can aid in determining if series terminating, pull-up, or pull-down resistors would be required when a system is designed.

The EE-Note is broken as follows: A table listing the I/O pins on the ADSP-21161, with a description of which pins contain internal keeper latches and pull-up/pull-down resistors. This is followed by a description of the internal keeper latch circuitry and the combined series resistance (internal & added resistance) of all I/O pins are discussed. Finally, we will examine each peripheral grouping on the ADSP-21161 and provide general recommendations for handling an unused pin in your system.

TABLE 1: ADSP-21161 I/O PINS

Pin Name	Type	Notes	Other Information
ADDR(23-0)	I/O/T		Keeper Latch (Only for ID = 00X)
DATA(47-16)	I/O/T		Keeper Latch (Only for ID = 00X)
MS~(3-0)	I/O/T		
RD~	I/O/T		20K Pull-Up (Only for ID = 00X)
WR~	I/O/T		20K Pull-Up (Only for ID = 00X)
BRST	I/O/T		Keeper Latch (Only for ID = 00X)
ACK	I/O/S		20K Pull-Up enabled during reset or when ID2-0 = 00X"
SBTS~	I/S		
CAS~	I/O/T		
RAS~	I/O/T		
SDWE~	I/O/T		
DQM	O/T		
SDCLK0	I/O/S/T		
SDCLK1	O/S/T		
SDCKE	I/O/T		
SDA10	O/T		
IRQ~(2-0)	I/A		
FLAG(11-0)	I/O/A		

TIMEXP	O		
HBR~	I/A		
HBG~	I/O		
CS~	I/A		
REDY	O(o/d)		
DMAR~(1-0)	I/A		20K Pull-Up (Only for ID= 00X)
DMAG~(1-0)	O/T		20K Pull-Up (Only for ID = 00X)
BR~(6-1)	I/O/S		
BMSTR	O		
ID(2-0)	I		
RPBA	I/S		
PA~	I/O/T		20K Pull-Up (Only for ID = 00X)
Dxy	I/O		50K Pull-Up
SCLKx	I/O		50K Pull-Up
FSx	I/O		
SPICLK	I/O		50K Pull-Up
SPIDS~	I		
MISO	I/O		50K Pull-Up
MOSI	I/O		50K Pull-Up
LxDAT(7-0)	I/O		50K Pull-Down
LxCLK	I/O		50K Pull-Down
LxACK	I/O	(1)	50K Pull-Down
EBOOT	I		
LBOOT	I		
BMS~	I/O/T		
CLKIN	I		
XTAL	O		
CLK_CFGx	I		
CLKDBL~	I		
CLKOUT	O/T		Keeper Latch (Only for ID = 00X)
RESET~	I/A		
TCK	I		
TMS	I/S		20K Pull-Up
TDI	I/S		20K Pull-Up
TDO	O		
TRST~	I/A		20K Pull-Up
EMU~	O(o/d)		50K Pull-Up

Notes:

- 1) When configured as DATA15-0, LKDATxy are I/O/T just like DATA47-16
- 2) ID=00X indicates the pull-ups and keeper latches are activated for processors hardwired as ID=0 in a single processor system or ID=1 in a multiprocessor system

ADSP-21161 I/O Pins Include 50 Ohm Internal Resistance

The ADSP-21161 DSP has very fast drivers on all output pins, therefore the edge rates are steep, even at low-speed clock rates (i.e., slow SCLK or SPICLK rates). To compensate for these faster edge rates with smaller 0.18 micron CMOS geometries, the ADSP-21161 I/O drivers have been modified to reduce undesirable transmission line effects when connecting to other devices. **Unlike all previous SHARC processors, the ADSP-21161 contains a total internal series resistance equivalent to 50 ohms on all I/O drivers (EXCEPT for the CLKIN and XTAL pins).** As shown in figure 1, the internal resistance in the driver is 10 Ohms, therefore the inclusion of an additional 40 ohm series resistor results in a total resistance of 50 Ohms. This 50-Ohm resistance perfectly matches the characteristic impedance of a transmission line. Notice that the ESD protection feedback path is only found in pins which are bi-directional. Pins listed as "O" (output) only, do not include this signal feedback (ESD protection) path.

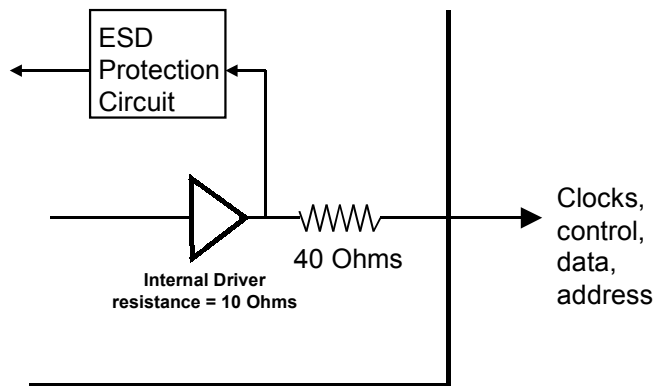


Figure 1: 50 Ohm Series Resistance in ADSP-21161 I/O Pins

The DSP hardware designer needs to be aware of the total 50 Ohm internal combined resistance of the DSP I/O pins, which then can remove the need for the designer to add external series terminating resistors in *point-to-point* DSP interconnections, such as the for link port signals between multiple SHARC DSPs. Therefore, for traces longer than 6 inches, external series resistors on control, data, clocks or frame sync pins are no longer required for point-to-point connections between SHARCs in order to dampen reflections which result from transmission-line effects. If the connection is to another device other than the ADSP-21161, then source termination is not required on the DSP pin, but a series resistor may still be required for the other device's pin, depending on its internal driver resistance. Note that for more complex trace interconnections (such as star configurations), termination techniques will still need to be employed in order to reduce ringing and reflections.

ADSP-21161 I/O Pins With Keeper Latches

As indicated in Table, 1, keeper latches are used on some ADSP-21161 pins when their corresponding ID2-0 pins are hardwired to either a 0 or a 1. A *Keeper latch* is a logic level hold circuit, and basically consists of a two weak inverter connected back to back. The Figure 2 below shows the basic concept of a keeper latch:

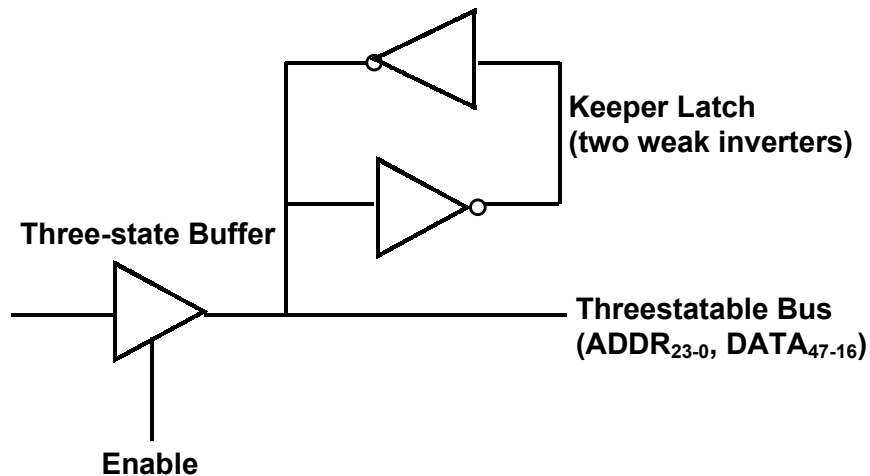


Figure 2. ADSP-21161 I/O drivers containing Keeper Latches

The three-state buffer is much stronger driver than the weak inverters used in the keeper so that it always drives the bus with the value that it intends to. But when the buffer is not driving, the weak inverter (A) keeps the bus at the same logic level that the buffer drove it to. Thus, keeper latches are used in the ADSP-21161 to ensure that the inputs of the TTL buffers do not float by simply keeping them to the last state in which the pin was driven, either high or low.

The following section contains recommendations for handling unused input pins, and is broken down into sections based on the ADSP-21161 SHARC DSP's peripheral functions. Within each category will be a list of each pin associated with the particular section, and the general recommendation for handling the pin if it will not be used in your system.

Link Ports

LxDAT₇₋₀, LxCCLK, LxACK: The link port data, clock and acknowledge lines all contain internal pull-down resistors, therefore they can be left floating if unused.

Serial Ports

DxA, Dx B, SCLKx: The serial port data and clock lines all contain 50 k-ohm internal pull-up resistors, therefore they can be left floating if unused.

FSx: The frame sync lines should be pulled or tied high if unused. Pulling or tying frame sync signals high will prevent unwanted power consumption if the serial ports are inadvertently enabled.

Serial Peripheral Interface

SPICLK, MOSI, MISO, SPIDS~: The serial peripheral interface clock (SPICLK), and data lines (MISO, MOSI) all contain 50 k-ohm internal pull-up resistors, therefore they can be left floating if unused.

SDRAM Interface

SDCLKx, SDCKE, SDWE~, CAS~, RAS~, DQM, SDA10: The SDRAM signals can be left floating if unused.

External Port Interface

ADDR₂₃₋₀, DATA₄₇₋₁₆ : The address, data and select lines can be left floating if unused.

REDY: The REDY line can be left floating because it is an output signal.

MS₃₋₀~: The memory select lines in a single processor system can be left floating as they are always outputs. In a multi-SHARC systems, the bus master drives the memory select lines, which are tracked by the slave SHARCs, so all memory select lines should be connected together.

RD~, WR~ : In the unusual case no host is driving read or write and the SHARC is not bus master the read and write lines should be pulled high. If the SHARC is the bus master the read and write lines can be left floating. (The master drives the read and write lines.).

ACK: In multiprocessor systems, the ACK signal is an input to the DSP bus master and does not float when it is not being driven. If the acknowledge signal will not be used, leave ACK floating. It is not necessary to use an external pullup resistor on the ACK line during booting or at any other time. The ACK pin is pulled high internally with a 20 kOhm equivalent resistor and is activated under the following conditions:

- when the DSP is in reset (regardless of hardwired ID pin configuration)
- After reset, in a single processor system (ID2-0=000)
- After reset, in a multiprocessing system, the processor with it's ID2-0 pins = 001

BRST: If the sequential burst access signal will not be used, leave BRST floating.

HBR~, CS~: If there is no host processor, host bus request and chip select should be pulled or tied high.

HBG~: In the unusual case the SHARC has an id greater than 1 and there is no bus master, the host bus grant line should be pulled high. If id is 1 or less and there will be no arbitration for the bus, host bus grant can be left floating.

BR₆₋₁: In a multiprocessor system pull the unused Bus Request pins high (the processor drives its own BRx line). If IDx=000 leave bus request pins floating.

DMA Handshaking Pins

DMAR1~, DMAR2~: If DMA request 1 and DMA request 2 will not be used pull the pins high. Pulling them high will prevent them from floating to a low logic level and interfering with DMA channels 10 and 11.

DMAG1~, DMAG2~: DMAG1 and DMAG2 are outputs and can be left floating if unused.

Misc I/O Control Pins

FLAG₁₁₋₀: The programmable I/O flag pins can be left floating if unused.

IRQ₂₋₀~: If the interrupt request lines are unused they should be pulled or tied high.

TIMEXP: Timer expired is an output and can be left floating if unused.

BMSTR: Bus Master Output is an output signal and can be left floating if unused.

JTAG

TRST~: The test reset pin must be asserted (pulsed) low after power up. If the JTAG emulator will not be used, the test reset pin must be tied low.

TCK: The test clock should be pulled or tied either high or low if the JTAG emulator will not be used.

TMS, TDI: The test mode select and test data input pins can be left floating if the JTAG emulation is not used. These pins have internal pull-up resistors.

TDO, EMU~: The test data output and emulation status pins can be left floating if JTAG emulation is unused. These signals are output only.

Miscellaneous

SBTS~: The suspend bus three state should be tied high if no other device will be connected and the pin is not used.

PA~: The core priority access pin can be left floating if unused. The PA is pulled high with an internal pull-up resistor.

BMS~: If the EPROM boot select pin (EBOOT) is tied to ground making BMS~ an input pin, i.e. EPROM boot is not selected, then the boot memory select pin must be tied low or high. If EBOOT is tied high, then BMS~ is an output.

XTAL: The Crystal Oscillator Terminal 2 pin (used in conjunction with CLKIN when using external crystals) must be left unconnected whenever an external clock oscillator is used (only CLKIN used). Do not pull or tie this pin high or low if it is not connected to an external crystal.

CLKOUT: The Local Clock Out should always be left unconnected when not used. Bit #22 (COD, CLKOUT disable) in the SYSCON register allows the user to three-state the CLKOUT pin.

NC: These pins are reserved and should always be left unconnected.

The remaining pins, which will be listed for completeness, are associated with functionality that *must* be used. The pins either configure a booting mode, supply internal and external supply voltages, signal grounds, input clock or reset. Please refer to the *ADSP-21161 SHARC DSP Hardware Reference Manual* or the *ADSP-21161 DSP Microcomputer Data Sheet* for the proper connection of the following pins: **ID₂₋₀**, **RPBA**, **EBOOT**, **LBOOT**, **CLK_CFG₁₋₀**, **CLKDBL~**, **CLKIN**, **RESET~**, **VDDINT**, **VDDEXT**, **AVDD**, **AGND** and **GND**.